AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a first element forming region of a main surface of a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over a second element forming region of said main surface of said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film being thinner than said first gate insulating film,

wherein said first gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film and having a thickness greater than that of said thermally oxidized film,

wherein said second gate insulating film includes a thermally oxidized film,

wherein a thickness of said thermally oxidized film of said first gate insulating film is thinner than that of said thermally oxidized film of said second gate insulating film,

wherein said first element forming region and said second element forming region are individually isolated by an element isolation region,

wherein said element isolation region is formed by forming grooves in said substrate, depositing an insulating film over said grooves by a vapor deposition method, and polishing said insulating film so as to fill said insulating film in said grooves, and

wherein said deposited film extends over said element isolation region such that an edge portion of said first gate electrode is formed over said deposited film at a portion of said deposited film positioned over said element isolation region.

2. (Previously Presented) A semiconductor integrated circuit device according to claim 1, wherein an etching rate of said insulating film filled in said groove is lower than that of said thermally oxidized film.

3. (Original) A semiconductor integrated circuit device according to claim 1, wherein said deposited film is formed by a vapor deposition method.

4. (Previously Presented) A semiconductor integrated circuit device according to claim 3, wherein said vapor deposition method is a chemical vapor deposition method.

5 – 55. (Cancelled)

56. (Previously Presented) A semiconductor integrated circuit device according to claim 1, wherein said element isolation region is an insulating region having a thickness greater than that of said first gate insulating film.

57. (Previously Presented) A semiconductor integrated circuit device according to claim 56, wherein said insulating film is integrally formed with an element isolation film defining a first MISFET forming region, and wherein an etching rate of said insulating film filled in said groove is lower than that of a thermally oxidized film.

58 -70. (Cancelled)